RECEIVED
CENTRAL FAX CENTER
JAN 30 2008

IN THE CLAIMS

1 (Previously Presented). A method comprising:

forming a phase change memory including a phase change storage element and a phase change threshold switch;

forming the phase change storage element and the phase change threshold switch within a memory area and providing a periphery beside said memory area, said periphery including no phase change memory elements; and

forming a damascene via to a conductive line in said periphery.

Claim 2 (Canceled).

3 (Previously Presented). The method of claim 1 including forming said switch over said element.

4 (Previously Presented). The method of claim 3 including forming, in said memory, a pore over a substrate, said pore having a dimension smaller than the feature size possible with lithographic techniques.

5 (Original). The method of claim 4 including forming said pore by forming an aperture through an insulator and forming a sidewall spacer in said aperture.

6 (Previously Presented). The method of claim 5 including forming a lower electrode of said phase change storage element in said pore.

7 (Previously Presented). The method of claim 1 including forming a barrier layer between said threshold switch and said storage element.

8 (Previously Presented). The method of claim 1 including forming an upper electrode over said phase change storage element, said upper electrode having a vertical extent at least twice its horizontal extent.

PAGE 3/6 * RCVD AT 1/30/2008 10:56:44 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-4/1 * DNIS:2738300 * CSID:7134688883 * DURATION (mm-ss):01-52

9 (Previously Presented). The method of claim 1 including forming an electrode over said phase change storage element, said electrode having sidewall spacers.

10 (Original). The method of claim 9 including using said sidewall spacers as a mask to etch through underlying layers.

11 (Previously Presented). The method of claim 1 wherein forming said phase change memory includes forming a memory array including a plurality of memory cells as a plurality of integrated islands spaced from one another.

12 (Original). The method of claim 11 including filling the regions surrounding said islands with an insulator.

13 (Previously Presented). The method of claim 12 including forming said insulator to a height over the upper extent of said islands.

14 (Previously Presented). The method of claim 13 including forming grooves through said insulator down to and past the upper extent of said islands.

15 (Currently Amended). The method of claim 13 including forming said insulator over the memory area and the periphery and forming a vertical groove in said insulator over said memory area ~~array~~ and a vertical groove in said insulator over [[in]] said periphery.

16 (Original). The method of claim 15 including filling said groove in said periphery with a sacrificial light absorbing material.

17 (Previously Presented). The method of claim 16 including etching said sacrificial light absorbing material in said groove in said periphery.

18 (Previously Presented). The method of claim 17 wherein forming said damascene via includes filling said groove in the periphery with a conductive material.

PAGE 4/6 * RCVD AT 1/30/2008 10:56:44 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-4/1 * DNIS:2738300 * CSID:7134688883 * DURATION (mm-ss):01-52

19 (Previously Presented). The method of claim 18 including forming said groove in said periphery deeper than said groove in the memory array.

20 (Previously Presented). The method of claim 19 including forming an upper electrode over said phase change storage element and forming said groove in said periphery to a depth below the upper extent of said upper electrode and below the lower extent of said upper electrode.

Claims 21-36 (Canceled).

PAGE 5/6 * RCVD AT 1/30/2008 10:56:44 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-4/1 * DNIS:2738300 * CSID:7134688883 * DURATION (mm-ss):01-52